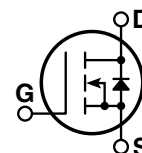
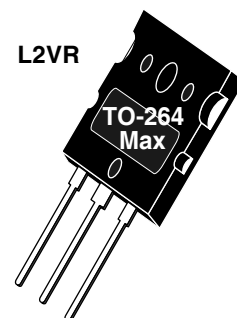


POWER MOS V® MOSFET

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.

- **TO-264 MAX Package**
- **Avalanche Energy Rated**
- **Faster Switching**
- **Lower Leakage**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT8018L2VR	UNIT
V_{DSS}	Drain-Source Voltage	800	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	43	Amps
I_{DM}	Pulsed Drain Current ^①	172	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	833	Watts
	Linear Derating Factor	6.67	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	43	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	3200	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	800			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 21.5A$)			0.180	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 800V, V_{GS} = 0V$)			25	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 640V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			250	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 5mA$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT8018L2VR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		10700		pF
C_{oss}	Output Capacitance			1180		
C_{rss}	Reverse Transfer Capacitance			610		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 400V$ $I_D = 43A @ 25^\circ C$		610		nC
Q_{gs}	Gate-Source Charge			60		
Q_{gd}	Gate-Drain ("Miller") Charge			360		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 400V$ $I_D = 43A @ 25^\circ C$ $R_G = 0.6\Omega$		19		ns
t_r	Rise Time			17		
$t_{d(off)}$	Turn-off Delay Time			80		
t_f	Fall Time			12		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			43	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			172	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V$, $I_S = -43A$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -43A$, $dI_S/dt = 100A/\mu s$)		930		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -43A$, $dI_S/dt = 100A/\mu s$)		29		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			10	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.15	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_J = +25^\circ C$, $L = 3.46mH$, $R_G = 25\Omega$, Peak $I_L = 43A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 43A$ $dI/dt \leq 700A/\mu s$ $V_R \leq 800V$ $T_J \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

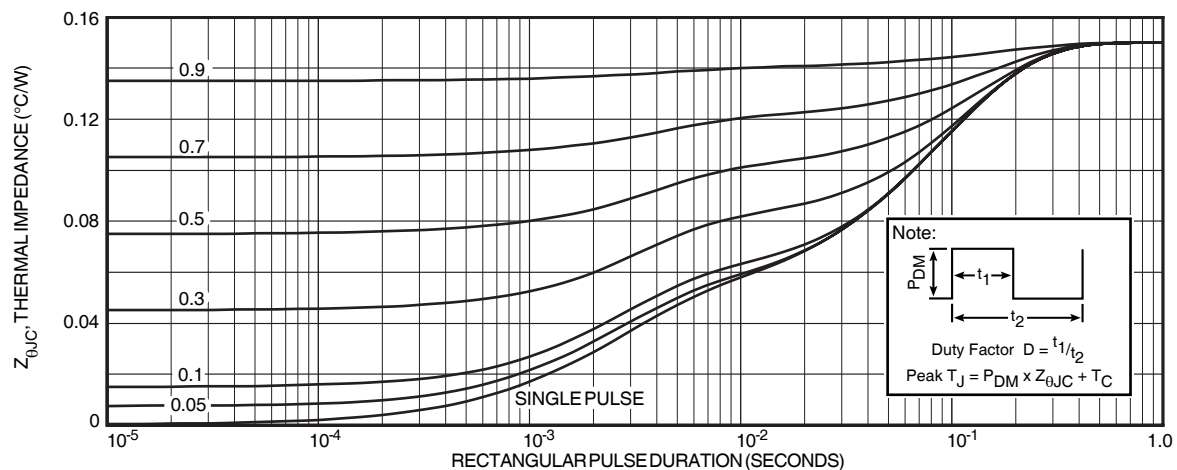


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

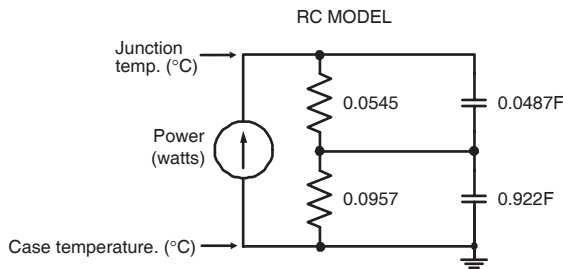


FIGURE2, TRANSIENT THERMAL IMPEDANCE MODEL

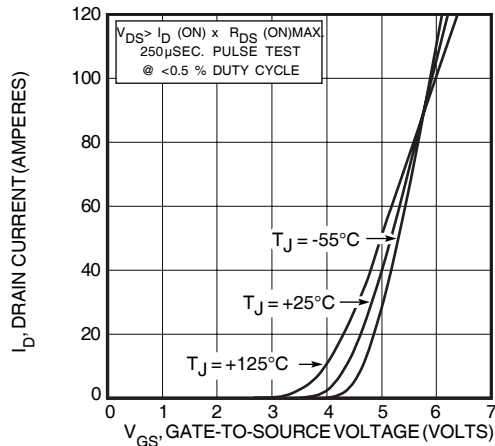


FIGURE4, TRANSFER CHARACTERISTICS

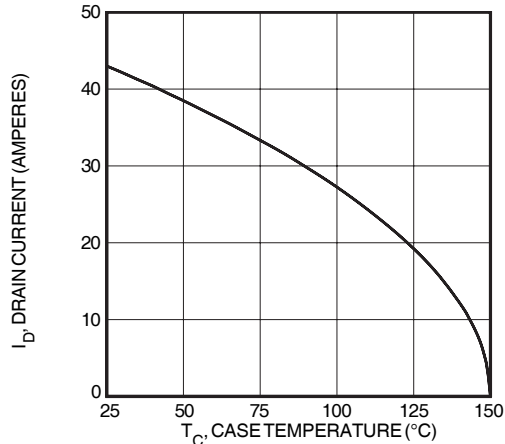


FIGURE6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

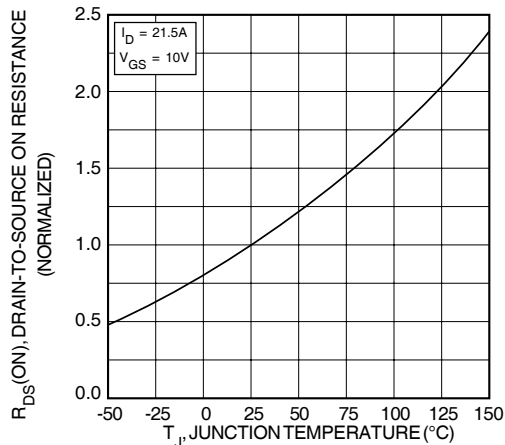


FIGURE8, ON-RESISTANCE vs. TEMPERATURE

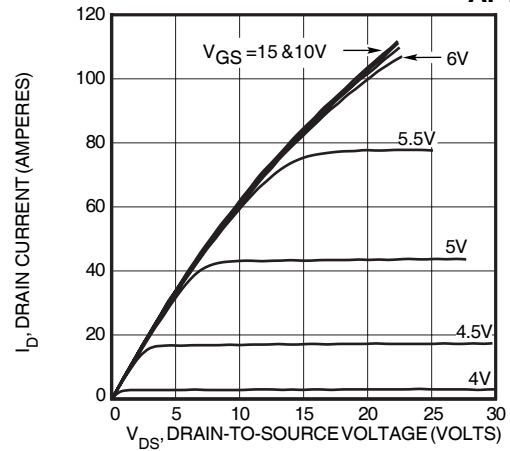


FIGURE3, LOW VOLTAGE OUTPUT CHARACTERISTICS

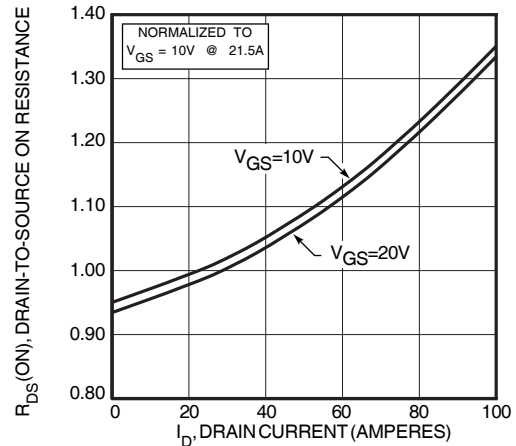


FIGURE5, $R_{DS(ON)}$ vs DRAIN CURRENT

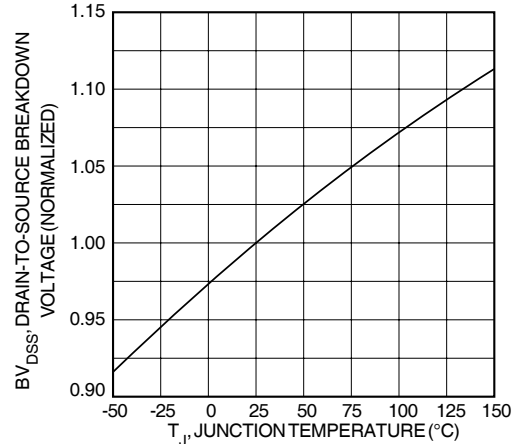


FIGURE7, BREAKDOWN VOLTAGE vs TEMPERATURE

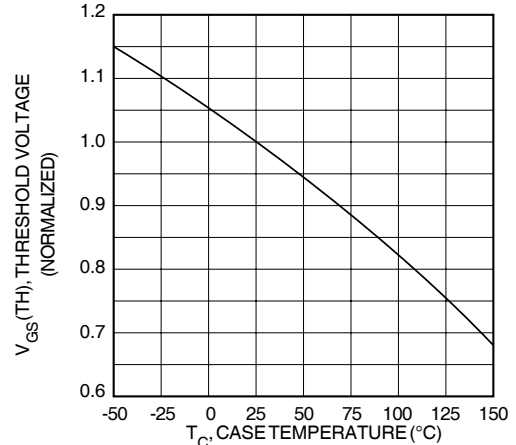


FIGURE9, THRESHOLD VOLTAGE vs TEMPERATURE

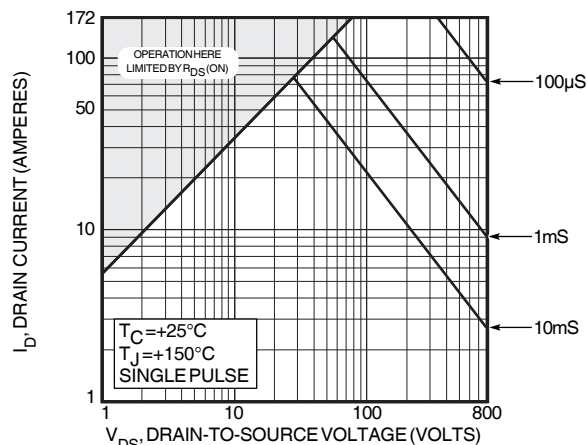


FIGURE 10, MAXIMUM SAFE OPERATING AREA

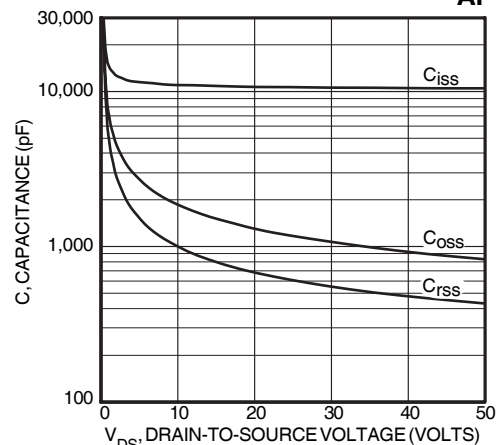


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

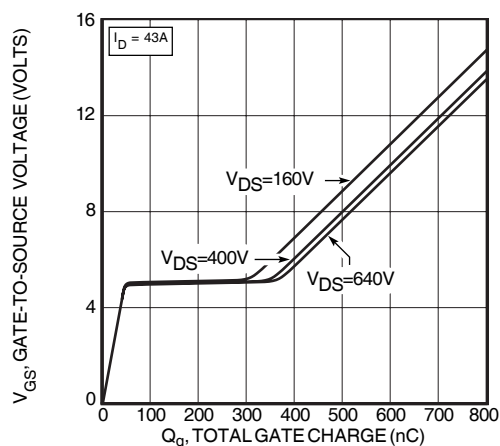


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

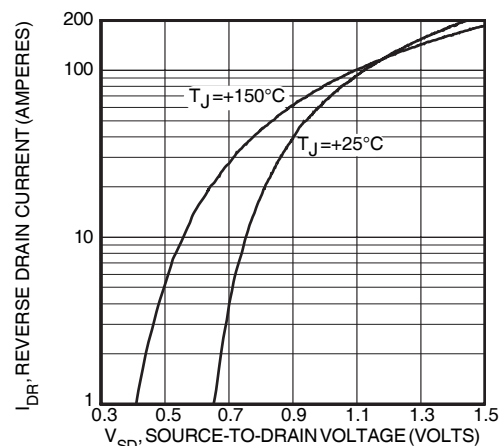
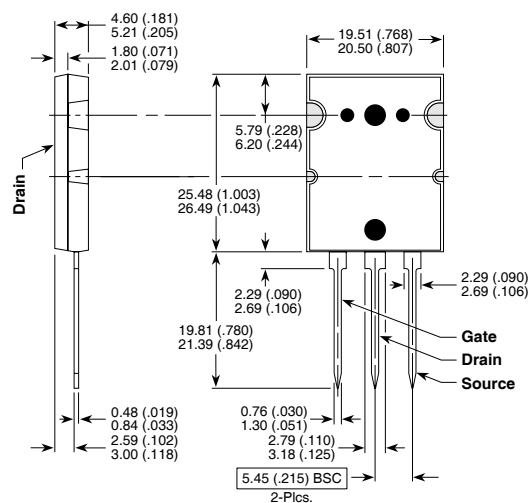


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-264 MAX™(L2) Package Outline (L2VR)



Dimensions in Millimeters and (Inches)

APT's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522

5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.